REMARKS

Claims 1-20 remain in the application, with claims 1-20 having been amended hereby.

The claims have been carefully reviewed and amended with particular attention to the points raised in the Office Action. It is submitted that no new matter has been added and no new issues have been raised by the present amendment.

Reconsideration is respectfully requested of the objections made to the disclosure as allegedly containing informalities. The instances noted in the Office Action have been addressed by the amendments made to the specification hereby.

Withdrawal of the objections to the disclosure is respectfully requested.

Reconsideration is respectfully requested of the rejection of claims 1, 3-5, 7, 9-11, 13-15, 17, and 19-20 under 35 U.S.C. § 102(e), as allegedly being anticipated by U.S. Patent No. 5,986,589 (Rosefield et al.).

Applicant has carefully considered the comments of the Office Action and the cited references, and respectfully submits that amended claims 1, 3-5, 7, 9-11, 13-15, 17, and 19-20 are patentably distinct over the cited reference for at least the following reasons.

The present invention relates to a digital signal processing system, method, and apparatus, suitably applicable to transmission of digital audio data, digital video data, etc. using the IEEE-1394 standard.

Rosefield et al., as understood by Applicants, relates to

a multi-stream audio sampling rate conversion circuit and method. The sample rate conversion system uses a digital signal processor (DSP) and a separate sample rate conversion circuit (SRC) to perform multiple-stream conversion and mixing of different rate input audio streams. The sample rate conversion system converts data such as multiple streams of digital audio data sampled at different rates, and performs interpolation, decimation, FIR filtering, and mixing of multiple streams of data using the separate SRC. The SRC uses two bidirectional I/O memories for alternately storing input and output data as part of a sample rate converter. When the sample rate converter writes output to one of the bidirectional memories, it has the option of summing the data with the data already stored in the same I/O memory to allow a separate digital signal processor to use the sample rate converter circuit to perform some of the mixing for the multiple streams.

The Office Action states that Rosefield et al. discloses, inter alia, a digital signal processor connected to a unit (e.g., the sample rate converter)(see Office Action, p. 3, lns. 1-6).

As understood by Applicants, the digitized input data streams from the audio sampling stage or from the host PCI bus are sent to the sample rate conversion system. The sample rate conversion system includes the digital signal processor and the sample rate converter circuit (see Rosefield et al., col. 3, ln. 53 to col. 4, ln. 3). The sample rate converter receives the plurality of input data streams from the digital

signal processor through bidirectional I/O memories (see id.).

It is respectfully submitted, however, that Rosefield et al. does not disclose a digital signal processing system including a first digital signal processing apparatus connected via a digital bus to a second digital signal processing apparatus whose data transmission rate can be controlled by other apparatuses on the digital bus, as recited in amended independent claim 1.

The Office Action further cites col. 3, ln. 53 to col. 4, ln. 29 of Rosefield et al. as allegedly disclosing that the unit (e.g., the sample rate converter) has a data transmission rate that can be externally controlled (see Office Action, p. 3, lns. 6-11).

The section of Rosefield et al. cited by the Office Action states that ''[t]he SRC 36 also includes a DSP multistream conversion interface 47 to facilitate conversion, mixing and communication with the DSP as further described below. Control logic 48 receives variable rate control data 50 from the DSP through the DSP multistream conversion interface 47 and alternately converts each of the plurality of input data streams to output data representing an input data stream as if it were sampled at a different rate based on the stored previous samples in the residue memory 42 for each input data stream'' (see Rosefield et al., col. 4, lns. 15-30).

It is respectfully submitted, however, that neither the cited section nor the remainder of Rosefield et al. disclose a first digital signal processing apparatus connected via a

digital bus to a second digital signal processing apparatus whose data transmission rate can be controlled by other apparatuses on the digital bus, as recited in amended independent claim 1.

Additionally, it is submitted that Rosefield et al. does not disclose generating means for generating a command for making an inquiry to the second digital signal processing apparatus about a capability of rate control functions, and that the predetermined digital bus supports real-time data transmission for transmitting audio/visual data and asynchronous data transmission for transmitting control data, as recited in amended independent claim 1.

It is respectfully submitted that Rosefield et al. does not disclose or suggest a digital signal processing system including a first digital signal processing apparatus connected via a predetermined digital bus to a second digital signal processing apparatus whose data transmission rate can be controlled by other apparatuses on the digital bus, the first digital signal processing apparatus comprising generating means for generating a command for making an inquiry to the second digital signal processing apparatus connected via the predetermined digital bus about a capability of rate control functions of the second digital signal processing apparatus, transmitting means for transmitting the command via the predetermined digital bus, and receiving means for receiving a response to the transmitted command, wherein the predetermined digital bus supports real-time data transmission for transmitting audio/visual data and

asynchronous data transmission for transmitting control data, and the second digital signal processing apparatus transmits the data via the predetermined digital bus, as described above and as recited in amended independent claim 1.

Accordingly, for at least the above-stated reasons, it is respectfully submitted that amended independent claim 1, and the claims depending therefrom, are patentable over the cited reference. Amended independent claims 5, 7, 11, 15, and 17, and the claims depending therefrom, are believed to be patentable over the cited reference for at least similar reasons.

Withdrawal of the rejection under 35 U.S.C. § 102(e) is respectfully requested.

Reconsideration is respectfully requested of the rejection of claims 2, 6, 8, 12, 16, and 18 under 35 U.S.C. § 103, as allegedly being unpatentable over Rosefield et al. in view of U.S. Patent No. 5,907,295 (Lin).

Applicant has carefully considered the comments of the Office Action and the cited references, and respectfully submits that amended claims 2, 6, 8, 12, 16, and 18 are patentably distinct over the cited references for at least the following reasons.

The Office Action notes that Rosefield et al. fails to disclose a synchronous control and a variable rate control for fine adjustment of a base data transmission rate (see Office Action, p. 9, lns. 2-4). Lin is cited as allegedly disclosing the missing element.

Lin, as understood by Applicants, relates to a system for

audio sample-rate conversion using a linear-interpolation stage with a multi-tap low-pass filter requiring reduced coefficient storage. Audio sample rates are converted by an arbitrary ratio of Q/P using a two-stage sample-rate converter. One stage is an L-tap low-pass finite-impulse-response (FIR) filter, while the other stage is a linear interpolator. Coefficient storage for the L-tap low-pass FIR filter is dramatically reduced by reducing the effective P factor by using two stages, with each stage adjusting the sampling rate by a different ratio. A first stage adjusts the sampling rate by Q0/P0, while a second stage further adjusts the sampling rate by Q1/P1. Q0 and P0 are large integers of about 400 to 700 that differ by one or three making the ratio Q0/P0 is very close to one. The linear interpolator stage eliminates or adds one or three samples and smoothes the samples by linear interpolation over the 400 to 700 remaining samples. The FIR filter stage adjusts the sample rate by a ratio of Q1/P1, which is approximately but not exactly Q/P. The FIR filter smoothes the expanded or reduced samples using weighting coefficients. Only P1 sets of coefficients are stored, rather than P sets.

It is respectfully submitted, however, that Lin does not disclose or suggest a digital signal processing system including a first digital signal processing apparatus connected via a digital bus to a second digital signal processing apparatus whose data transmission rate can be controlled by other apparatuses on the digital bus, or generating means for generating a command for making an

inquiry to the second digital signal processing apparatus about a capability of rate control functions, as recited in amended independent claim 1.

It is respectfully submitted that neither Rosefield et al. nor Lin, alone or in combination, disclose or suggest a digital signal processing system including a first digital signal processing apparatus connected via a predetermined digital bus to a second digital signal processing apparatus whose data transmission rate can be controlled by other apparatuses on the digital bus, the first digital signal processing apparatus comprising generating means for generating a command for making an inquiry to the second digital signal processing apparatus connected via the predetermined digital bus about a capability of rate control functions of the second digital signal processing apparatus, transmitting means for transmitting the command via the predetermined digital bus, and receiving means for receiving a response to the transmitted command, wherein the predetermined digital bus supports real-time data transmission for transmitting audio/visual data and asynchronous data transmission for transmitting control data, and the second digital signal processing apparatus transmits the data via the predetermined digital bus, as described above and as recited in amended independent claim 1.

Accordingly, for at least the above-stated reasons, it is respectfully submitted that amended independent claim 1, and the claims depending therefrom, are patentable over the cited references. Amended independent claims 5, 7, 11, 15, and 17,

and the claims depending therefrom, are believed to be patentable over the cited references for at least similar reasons.

Furthermore, it is respectfully submitted that there is no motivation within the cited references to combine the elements in the manner suggested in the Office Action.

Withdrawal of the rejection under 35 U.S.C. § 103(a) is respectfully requested.

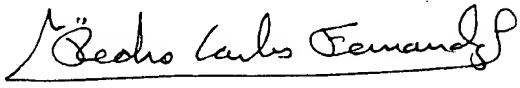
Should the Examiner disagree, it is respectfully requested that the Examiner specify where in the cited document there is a basis for such disagreement.

The references made of record have been reviewed but are not seen to disclose or suggest the present invention as recited in the amended claims.

The Office is hereby authorized to charge any fees which may be required in connection with this amendment and to credit any overpayment to Deposit Account No. 03-3125.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,
COOPER & DUNHAM, LLP



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